In the United States Patent and Trademark Office

In re the Application of:
Lee D. Whetsel TI-14124D.5

Div. of Serial No: 10/649,274 Prev. Art Unit: 2131

Filed: herewith Prev. Examiner: Hua, Ly

Title: Digital Bus Monitor Integrated Circuits

Petition to Make Special
Under 37 CFR 1.102 and
MPEP section 708.02, Paragraph VIII

October 21, 2003

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as Express Mail airbill #EV33320884 in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 21, 2003

Lawrence J. Bassuk, Reg. No. 29,043

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Petition With Fee

Applicant submits this petition to make special accompanied by the fee set forth in 37 CFR 1.17(h).

Please charge the fee under 37 CFR 1.17(h) of $130.00 to the deposit account of Texas Instruments Incorporated, Account No.20-0668.

Claims Directed To Single Invention

The accompanying Preliminary Amendment A presents claims directed to a single invention.

Statement of Pre-Examination Search Performed

Applicant submits a copy of two pre-examination search report letters, dated August 26, 2003 and September 15, 2003, from an Arlington, Virginia search firm.

Each letter lists the subject matter of the search, lists the references discovered, and lists the field of search. Each letter further indicates that an examiner confirmed the subclasses for searching, and that a computer search was performed on the EAST™ database at the USPTO.

The letters state no cut-off date for locating art. Some of the listed art was published after or has an effective art date after the effective filing date of this application, June 30, 1989.

Submission of Most Closely Related References

Each search report letter lists the art located in that search.

The electronically filed Information Disclosure Statement A (IDS-A) and accompanying PTO-1449 forms list US patents and US Patent Application Publications located in the pre-examination searches. The electronically filed IDS-A papers also list US patents of the present named inventor, and US patents and US Patent Application Publications cited in corresponding and other patent applications of the present named inventor. Under the new rules, applicant does not submit any copies of the US patents or US Patent Application Publications cited in the electronically filed IDS-A.

An enclosed paper IDS-A and PTO-1449 forms list Foreign Patent Documents and Other Documents cited in corresponding and other patent applications of the present named inventor; applicant encloses a copy of each listed reference.

Detailed Discussion of References

Applicant relies upon the combination of all the limitations in the independent claims for patentability and not just the preceding general description.

Independent claims 25 and 41 distinguish over the art by requiring: scanning a first signal into a serial scan path in response to a scan clock signal and a mode signal, storing the first signal, which indicates a desired protocol; comparing operating signals of functional circuits to compare signals; generating or detecting an event signal indicating a match; and performing a circuit operation on the integrated circuit using the desired protocol.

The following cited art fails to disclose scanning and storing a first signal indicating a desired protocol in an integrated circuit and performing a circuit operation using the desired protocol in response to an event signal, in the defined combinations.

Applicant could repeat a statement of these distinguishing limitations after the discussion of each following cited patent to meet the requirements of 37 CFR 1.111(b) and (c). Since each cited patent and the cited patents in combination fail to teach or suggest these distinguishing limitations, applicant will rely upon the preceding statement of the distinguishing limitations, without repetition.

US Patents

US 3,633,100 to Heilweil, et al., discloses applying two binary levels and an intermediate level of inputs to binary logic under test and to simulation logic. The outputs of the circuit under test and the simulation logic are compared to ascertain a good circuit

US 3,651,315 to Collins discloses a digital inspection system. The outputs from a product under test are compared with the outputs of a known good unit.

US 3,657,527 to Kassabgi, et al., discloses a system for automatically checking boards bearing integrated circuits. A program card is read automatically to provide both test input signals to the board and simulation output signals representative of the correct output signals.

US 4,642,561 to Groves, et al., discloses compressing the amount of data stored in local test data RAMs for implementing a circuit test.

US 4,857,835 to Whetsel discloses a global event qualification system. The system provides the timing and control required to activate an IC's test logic during normal functional operation. The input and outputs of an IC are bordered by unique comparator cells or Event Qualifier Cells (EQCELL). The EQCELLs compare the data entering or leaving the IC to test data vectors loaded during a scan operation. The EQCELL generates a control signal when the comparison is true.

US 4,864,570 to Savaglio, et al. discloses a processing pulse control circuit for use in treating indeterminate signature increments in an apparatus producing RPT signature analysis of digital circuits. A memory stores clock count values where indeterminate signature increments will be encountered.

US 4,872,169 to Whetsel discloses a hierarchical scan selection system. A serial scan path can be compressed or expanded to pass only through the desired logic element(s) to be tested.

US 5,054,024 to Whetsel was filed August 9, 1989 and is not prior art.

US 5,056,093 to Whetsel has the same disclosure as US 5,054,024 to Whetsel, was filed August 9, 1989, and is not prior art.

US 5,173,906 to Dreibelbis, et al., was filed August 31, 1990 and is not prior art to the present application.

US 5,353,308 to Whetsel has an effective filing date of August 6, 1990 and is not prior art.

US 5,623,500 to Whetsel has the same disclosure as US 5,353,308 to Whetsel, has an effective filing date of August 6, 1990, and is not prior art.

US 5,677,915 to Whetsel has an effective filing date of August 18, 1993 and is not prior art.

US 6,158,035 to Whetsel has an effective filing date of March 30, 1990 and is not prior art.

US 5,958,072 to Jacobs, et al., was filed January 13, 1997 and is not prior art to the present application.

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Conclusion

The claims distinguish over the cited art. The specification and claims are in allowable form. Applicant requests allowance of the application.

Respectfully submitted,

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
972-917-5458

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Respectfully submitted,

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

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August 26, 2003

VIA FEDEX

Frank D. Cimino, Esq.
TEXAS INSTRUMENTS
7839 Churchill Way
Mail Station 3999
Dallas, TX 75251

RE: PROTOCOL PROCESS CLAIMS
Your Ref. No.: TI-14124D.3 Claim Set 1
Our Docket/Invoice No.: 30786.TI

Dear Frank:

In response to your search request on August 12, 2003, we performed the patentability search you requested. The following is a complete report of our search parameters and findings for discovered references.

SUBJECT MATTER OF SEARCH

In our search, we focused broadly on a process of operating an integrated circuit comprising:

A. Scanning a fist signal into a serial scan path on the integrated circuit in response to a scan clock signal and a scan mode signal;

B. Storing the first signal in a register on the integrated circuit, the register being coupled to the scan path on the integrated circuits, the first signal indicating a desired protocol;

C. Operating functional circuits on the integrated circuit to produce operating signals;

D. Comparing, on the integrated circuit, the operating signals to compare signals stored in an expected data memory, on the integrated circuit;

E. Generating an event signal on the integrated circuit, when the operating signals match the compare signals; and

F. In response to the event signal, performing a circuit operation on the integrated circuit using the desired protocol.

REFERENCES DISCOVERED

2001/0049803	Kurafuji
2003/0005379	Slawecki et al.
5,958,072	Jacobs et al.
4,872,169	Whetsel, Jr.
2003/0033556	West
2003/0014704	Nishimura
2002/0199143	Alt et al.
2002/0133774	Inuoe
6,158,035	Whetsel, Jr. et al.
5,677,915	Whetsel
5,623,500	Whetsel, Jr.
5,353,308	Whetsel, Jr.
5,173,906	Dreibelbis et al.
5,056,093	Whetsel
5,054,024	Whetsel
4,857,835	Whetsel, Jr.

DISCUSSION OF REFERENCES

Kurafuji discloses microprocessor internally provided with test circuit, which includes programs counter setting register, a comparator and a test-event signal (See Abstract and Claims).

Slawecki et al. disclose a comparison method and apparatus, which includes at least one scan latch, a memory unit and a comparison circuit (See Abstract and Claims).

Jacobs et al. disclose a processor-to-memory-bus interface for a computer system having test-event hardware, which includes test-event generator, timing generator and test-event selector (See Figures and Claims 1, 6).

Whetsel, Jr. discloses a method of testing circuitry having a serial scan path through a logic circuit (See Figures and Claim 1).

The remaining references are cited as of interest and are submitted for your review.

FIELD OF SEARCH

CLASS	SUBCLASS
714	25, 30, 724, 726, 733, 734, 736

In addition to a complete search of the above subclasses, confirmed by Primary Examiner Stephane Dildine, Jr. of Group 2100, an extensive computer search was performed on the EAST® database at the USPTO, utilizing the submitted disclosure materials and our formulated search methods derived therefrom.

Enclosed are copies of the cited references and our invoice for services rendered and disbursements for this matter.

In closing, we would like to thank you for giving us this opportunity to serve you. If there are any questions or comments concerning this search or our services, please contact us at your earliest convenience.

Sincerely,

Tuan Nguyen

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PATENT AND TRADEMARK PROFESSIONAL SERVICES
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Crystal Plaza One
2001 Jefferson Davis Highway
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703-412-4866 phone
703-412-4884 fax
www.e-pat.com

September 15, 2003

VIA FEDEX

Frank D. Cimino, Esq.
TEXAS INSTRUMENTS
7839 Churchill Way
Mail Station 3999
Dallas, TX 75251

RE: PROTOCOL PROCESS CLAIMS
Your Ref. No.: TI-14124D.3 Claim Set 1
Our Docket/Invoice No.: 30786A.TI

Dear Frank:

In response to your email request on September 11, 2003, we performed the expanded patentability search you requested. The following is a complete report of our search parameters and findings for discovered references.

SUBJECT MATTER OF SEARCH

In our search, we focused broadly on a process of operating an integrated circuit comprising:

A. Scanning a fist signal into a serial scan path on the integrated circuit in response to a scan clock signal and a scan mode signal;

B. Storing the first signal in a register on the integrated circuit, the register being coupled to the scan path on the integrated circuits, the first signal indicating a desired protocol;

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D. Comparing, on the integrated circuit, the operating signals to compare signals stored in an expected data memory, on the integrated circuit;

E. Generating an event signal on the integrated circuit, when the operating signals match the compare signals; and

F. In response to the event signal, performing a circuit operation on the integrated circuit using the desired protocol.

ADDITIONAL REFERENCES DISCOVERED

4,865,570	Savaglio et al.
4,642,561	Groves et al.
3,657,527	Kassabgi et al.
3,651,315	Collins
3,633,100	Heilweil et al.

DISCUSSION OF REFERENCES

The references are cited as of interest and are submitted for your review.

FIELD OF SEARCH

CLASS	SUBCLASS
714	25, 30, 724, 726, 733, 734, 736

In addition to a complete search of the above subclasses, confirmed by Primary Examiner Stephane Dildine, Jr. of Group 2100, an extensive computer search was performed on the EAST® database at the USPTO, utilizing the submitted disclosure materials and our formulated search methods derived therefrom.

Enclosed are copies of the cited references and our invoice for services rendered and disbursements for this matter.

In closing, we would like to thank you for giving us this opportunity to serve you. If there are any questions or comments concerning this search or our services, please contact us at your earliest convenience.

Sincerely,

Tuan Nguyen